

NOTE:

1. 17 MIL TRACES ON L1 AND L6 LAYER ARE 50 OHMS +/- 10%
2. ALL VIA HOLES NEED TO BE TENTED ON TOP AND BOTTOM SIDE.
3. VIA HOLES UNDER IC U2 NEED TO BE FILLED WITH SOLDER MASK TO PREVENT SOLDER PASTE FLOW INTO VIAS.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.50mil	3.5	
3	L1_Top Layer	Copper	1.40mil		
4	Dielectric 1		8.50mil	4.7	
5	L2_GND1	Copper	1.40mil		
6	Dielectric 2		14.00mil	4.7	
7	L3_Signal	Copper	1.40mil		
8	Dielectric 3		8.50mil	4.7	
9	L4_Plane	Copper	1.40mil		
10	Dielectric 4		14.00mil	4.7	
11	L5_GND2	Copper	1.40mil		
12	Dielectric 5		8.50mil	4.7	
13	L6_Bottom Layer	Copper	1.40mil		
14	Bottom Solder	Solder Resist	0.50mil	3.5	
15	Bottom Overlay				

DESIGN INFORMATION	
MIN. TRACK WIDTH:	5 MIL
MIN. CLEARANCE:	5 mil
MIN. VIA PAD SIZE:	18 MIL
MINIMUM ANNULAR RING IPC Class 2 specifications	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408 <input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER 370HR	
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL +/-10% <input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS: <input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER	
BOARD FINISH:	
SILKSCREEN: <input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM	
SILKSCREEN COLOR: <input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER	
SOLDER RESIST COLOR: <input type="checkbox"/> GREEN <input checked="" type="checkbox"/> OTHER RED	
<input type="checkbox"/> MATTE <input checked="" type="checkbox"/> SEMI-GLOSS	
SURFACE FINISH: <input type="checkbox"/> IMMERSION GOLD (ENIG) <input checked="" type="checkbox"/> ENEPIG	
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER	
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRIM PER M1 BOARD OUTLINE
<input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3	
<input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE:
ADC3644 EVM

DESIGNED FOR:
Public Release

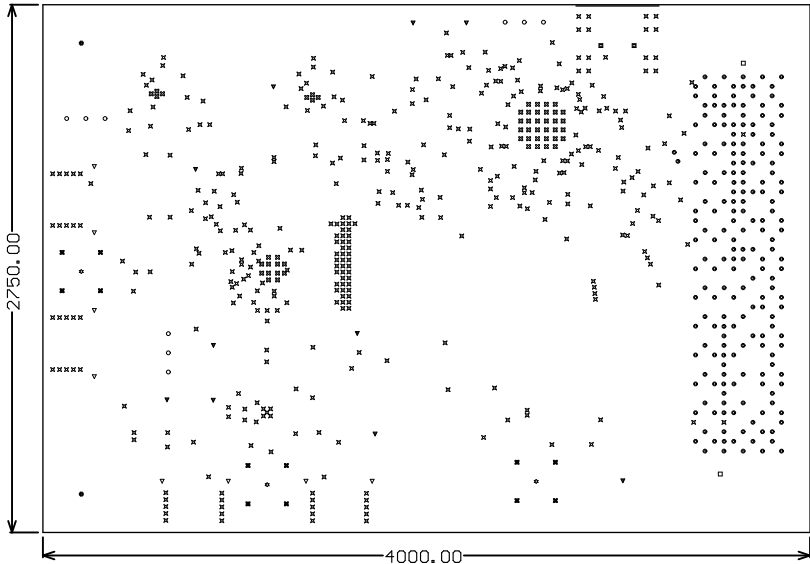
FILE NAME:
DC092A_PCB.PcbDoc

ENGINEER:
Daniel Brock

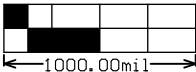
LAYOUT BY:
Daniel Brock

SCALE: 1.00

ALTUM DESIGNER VERSION:
18.1.9.240



Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Routed Path Length	Hole Length	Drill Layer Pair	Tolerance
⬜	2	35.43mil (0.900mm)	NPTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
⬜	2	50.00mil (1.270mm)	NPTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
⊗	52	7.87mil (0.200mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	+/- 3 mil
⊗	390	8.00mil (0.203mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
⊗	191	10.00mil (0.254mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	+/- 3 mil
▽	8	18.00mil (0.457mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
○	9	35.00mil (0.889mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
☆	3	59.06mil (1.500mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
▽	10	63.00mil (1.600mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	+/- 3 mil
⊗	12	66.93mil (1.700mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
⊗	2	125.98mil (3.200mm)	PTH	Round	-	-	L1_Top Layer - L6_Bottom Layer	
	681 Total							



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: DC092A	REV: A	SUN REV: Not In VersionControl
LAYER NAME = DC092A_PCB	TID #: N/A		
PLOT NAME = DC092A	GENERATED : 7/9/2019 1:17:22 PM	TEXAS INSTRUMENTS	

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